CLAIMS

1. A commutation and velocity control system of a brushless DC motor that receives a velocity command signal and provides command signals to drive the brushless DC motor, said system comprising:

a summer that receives the velocity command signal and a velocity feedback signal and provides a velocity error signal indicative of the difference;

a velocity loop compensator that receives said velocity error signal and provides a compensated velocity error signal;

a magnitude sensing circuit that senses the magnitude of said compensated velocity error signal and provides a velocity magnitude signal indicative thereof;

a polarity sensing circuit that senses the polarity of the said compensated velocity error signal and provides a velocity polarity signal indicative thereof;

an integrated circuit that includes

A) a velocity calculation circuit that receives a first sampled digitized signal indicative of resolver position at a first time and a second sampled digitized signal indicative of resolver position at a second time, and determines velocity based upon the difference between said first and second sampled digitized signals and provides a sensed digitized velocity signal indicative thereof;

B) a commutation logic circuit that receives said first sampled digitized signal, said velocity magnitude signal and said velocity polarity signal, and provides said command signal;

C) a counter that receives a signal indicative of said sensed digitized velocity signal

and provides a pulse width modulated output signal indicative thereof; and

a filter that receives said pulse width modulated output signal and generates said velocity feedback signal.

2. The commutation and velocity control system of claim 1, wherein said integrated circuit is configured as a field programmable gate array (FPGA).

3. The commutation and velocity control system of claim 2, further comprising:

a bridge circuit that receives a sine signal component and a cosine signal component from a resolver, and generates a first resolver signal and a second resolver signal separated by $(2*\theta)$, where θ is indicative of a resolver electrical angle;

wherein said FPGA comprises

a counter that receives said a first resolver signal and a second resolver signal and generates a count signal indicative of resolver position;

a first latch that receives said count signal and generates said first sampled digitized signal;

a second latch that receives said count signal and generates said first sampled digitized signal; and

a summer that computes the difference between said first and second sampled digitized signal and provides said sensed digitized velocity signal.

4. The commutation and velocity control system of claim 3, wherein said FPGA

comprises an up/down counter that cycles back and forth between zero counts and a fixed count value and provides a cycling count signal.

5. The commutation and velocity control system of claim 4, wherein said magnitude sensing circuit comprises:

a digital-to-analog converter that receives said cycling count signal and provides an triangular waveform signal; and

a first comparator that receives said triangular waveform signal and said compensated velocity signal and provides said velocity magnitude signal as a pulse width modulated signal whose duty cycle is indicative of the magnitude of the velocity.

6. The commutation and velocity control system of claim 5, wherein said polarity sensing circuit comprises:

a second comparator that receives said compensated velocity signal and provides said velocity polarity signal as a Boolean signal whose value is indicative of the polarity of said compensated velocity signal.

7. The commutation and velocity control system of claim 6, comprising a H-bridge driver circuit that includes a plurality of FETs responsive to said command signals to drive the brushless DC motor.

8. A commutation and velocity control system of a brushless DC motor that receives a

velocity command signal and provides command signals to drive the brushless DC motor, said system comprising:

a summer that receives the velocity command signal and a velocity feedback signal and provides a velocity error signal indicative of the difference;

means responsive to said velocity error signal for providing a compensated velocity error signal;

means for sensing the magnitude of said compensated velocity error signal and for provides a velocity magnitude signal indicative thereof;

means for sensing the polarity of the said compensated velocity error signal and for providing a velocity polarity signal indicative thereof;

an integrated circuit that includes

A) means for receiving a first sampled digitized signal indicative of resolver position at a first time and a second sampled digitized signal indicative of resolver position at a second time, and for determining velocity based upon the difference between said first and second sampled digitized signals, and for providing a sensed digitized velocity signal indicative thereof;

B) commutation logic means that receives said first sampled digitized signal, said velocity magnitude signal and said velocity polarity signal, for providing said command signal;

C) means responsive to a signal indicative of said sensed digitized velocity signal and for providing a pulse width modulated output signal indicative thereof; and

a filter that receives said pulse width modulated output signal and generates said

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